PPSC Computer Science Full Book test

Sr	Questions	Answers Choice
1	Which register is connected to the memory by way of the address bus.	A. MAR B. MDR C. SAM D. None
2	Which bus plays a crucial role in I/O	A. System bus B. Control bus C. address bus D. Both a and b
3	Which microprocessor to read an item from memory.	A. VAM B. SAM C. MOC D. None
4	VAM sand for	A. Valid memory address B. Virtual memory address C. variable memory address D. None
5	MAR stand for	A. Memory address register B. Memory data recode C. Micro data register D. None
6	SAM stand for	A. Simple architecture machine B. Solved architecture machine C. Both a and b D. None
7	Which register is used to communicate with memory.	A. MAR B. MDR C. Both a and b D. None
8	A microprocessor retries instructions from	A. Control memory B. Cache memory C. Main memory D. Virtual memory
9	The problems of bus confit and spares address distribution are eliminated by the use of ___ address technique.	A. Fully decoding B. Half decoding C. Both a and b D. None
10	in linear decoding address bus of 16 -bit wide can connect only of RAM	A. Address map is not contiguous B. Confects occur if two of the select lines become active at the same time C. If all unused address lines are not used as chip selectors then these unused lines become don't cares. D. None
11	Which storage technique does not decoding circuit.	A. Linear decoding B. Fully decoding C. partially D. None
12	The capacity of this chip is 1 KB they are organized in the form of 1024 words with 8 bit word the what is the site of address bus.	A. 8 bit B. 10 bit C. 12 bit D. 16 bit
13	When CS_ the chip is not selected at all hence D7 to D0 are driven to high impendence state.	A. High B. Low C. Medium D. Stand by
14	WE stand for	A. Write enable B. Wrote enable C. Write envy D. None
		A. Cable select

15	CS stand for	B. Chip select C. Control select D. Cable system
16	Which technique is uses for main memory array design.	A. Linear decoding B. Fully decoding C. Both a and b D. None
17	Which statement is false about WR signal	A. WR signal controls the input buffer B. the bar over Wr means that this is an active low signal C. the bar over WR means that this is an active high signal D. If WR is 0 then the input data reaches the latch input.
18	Which latch is mostly used creating memory register.	A. SR-Latch B. JK- Latch C. D-Latch D. T-Latch
19	Which RAM is created using MOS transistors.	A. Dynamic RAM B. Static RAM C. Permanent RAM D. SD RAM
20	Which type of RAM need regular referred.	A. Dynamic RAM B. Static RAM C. Permanent RAM D. SD RAM
21	The ram which is created using bipolar transistors is called.	A. Dynamic RAM B. Static RAM C. Permanent RAM D. DDR RAM
22	Customized ROMS are called.	A. Mask ROM B. Flash ROM C. EPROM D. None
23	Secondary memory is also called.	A. Auxiliary B. Backup store C. Both a and b D. None
24	Secondary memory can store.	A. Program store code B. Compiler C. Operating system D. All of these
25	Which is the type of microcomputer memory	A. Processor memory B. Primary memory C. Secondary memory D. All of these
26	Each memory location has	A. Address B. Contents C. Both a and b D. None
27	PROM stand for	A. Programmable Read only memory B. Erasable programmable read only memory C. Both a and b D. None
28	Using 12 binary digits how many queue house addresses would be possible.	A. 2⁸= 256 B. 2¹² = 4096 C. 2¹⁶ = 65536 D. None
29	When memory write or I/O read are active data is from the processor.	A. Input B. Out put C. Processor D. None
30	Which memory read or I/O read are active data is to the procesor.	A. Input B. Out put C. Processor D. None