PPSC Computer Science Full Book test

Sr	Questions	Answers Choice
1	How many type of cache memory	A. 1 B. 2 C. 3 D. 4
2	The amount of information which can be plead at one time in the cache memory is called.	A. Circle size B. Line size C. Wide line size D. None
3	The cache usually gets its data from the _____ whenever the instruction or data is required by the CPU.	A. Main memory B. Case memory C. Cache memory D. All of these
4	Which is the small amount of highs speed memory used to work directly with the microprocessor	A. Cache B. Case C. Cost D. Coos
5	_____is usually the first level of memory access by the microprocessor.	A. Cache memory B. Data memory C. Main memory D. All of these
6	The offset of a particular segment varies from_____	A. 000H to FFFH B. 0000H to FFFFH C. 00H to FFH D. 00000H to FFFFFH
7	_____ is the most important segment and it contains the actual assembly language instruction to be executed by the microprocessor.	A. Data segment B. Code segment C. Stack segment D. Extra segment
8	Which are the general register.	A. AX.; Accumulator B. BX: base C. CX: Count D. All of these
9	Which are the categorized of Flag	A. Conditional flag B. Control flag C. Both a and b D. None
10	AL stand for	A. Accumulator low B. Address low C. Appropriate low D. Application low
11	NMI stand for	A. Non mask able interrupt B. Non mistake interrupt C. Both a and b D. None
12	ALE stand for	A. Address latch enable B. Address light enable C. Address lower enable D. Address last enable
13	SI Stand for	A. Stand Index B. Source index C. Segment index D. Simple index
14	DI stand for	A. Destination index B. Defect index C. Definition index D. Delete index
15	BP stand for	A. Bit pointer B. Base pointer C. Bus pointer D. Byte pointer

16	SBA stand for	A. Segment bus address B. Segment not address C. Segment base address D. Segment byte address
17	PA stand for	A. Project address B. Physical address C. Pin address D. Pointer address
18	DIP stand for	A. Deal inline package B. Dual inline package C. Direct inline package D. Digital inline package
19	The pin configuration of 8086 is available in the.	A. 40 pin B. 50 pin C. 30 pin D. 20 pin
20	To provide clarity in case of the status register_____ and __ placeholders are displayed.	A. Binary B. Hexadecimal C. Both D. None
21	The _____ ddress of a memory is a 20 bit address for the 8086 microprocessor.	A. Physical B. Logical C. Both a and b D. None
22	The physical address of memory is.	A. 20 bit B. 16 bit C. 32 bit D. 64 bit
23	The size of each segment in 8086 is	A. 64 Kb B. 24 kb C. 50 kb D. 16 kb
24	How many types of addressing in memory.	A. Logical address B. Physical address C. Both a and b D. None
25	Which flag are used to record specific characteristics of arithmetic and logical instructions.	A. The stack B. The stand C. The status D. The queue
26	Which register contains the 8086/8088 flag	A. Status register B. Stack register C. Flag register D. Stand register
27	Which is the great importance's in modular programming	A. Stack segment B. Array segment C. Queue segment D. All of these
28	The lower and bit are called.	A. AL B. CL C. BL D. DL
29	The upper 8 bit are called.	A. BH B. AH C. BL D. DL
30	The accelerator is 16bit wide and is called.	A. AX B. AH C. AL D. DL