PPSC Computer Science Full Book test

Sr	Questions	Answers Choice
1	IRR stand for	A. Interrupt request register B. Input request register C. Input resolver register D. Interrupt resolver register
2	EOC stand for	A. End of conversion B. Emphasize of conversion C. End of controller D. None
3	INTR it implies the ___ signal	A. Interrupt request B. Interrupt Right C. Interrupt Rough D. interrupt Reset
4	Which is responsible for all the outside world communication by the microprocessor.	A. BIU B. PIU C. TIU D. LIU
5	Cache can be controlled.	A. 16 KB - 2MB B. 17 KB - 2MB C. 18 KB - 2 MB D. 19 KB - 2MB
6	Which are the cache controller ports.	A. 64 bit AHB -Lite slave ports B. 64- bit AHB -Lite Master ports C. Both a and b D. None
7	Which causes the microprocessor to immediately terminate its present activity.	A. RESET Signal B. INTERUPT signal C. Both D. None
8	Which formula is used to calculate the number of write stall cycles.	A. Reads * read miss rate* read miss penalty B. write * write miss + Write buffer stalls C. Memory access* cache miss rate * cache miss penalty D. None
9	Which formula is used to calculate the number of read stall cycles.	A. None B. Reads read miss rate read miss penalty C. Write +Wrier buffer stalls D. Memory access* cache miss rate * cache miss penalty
10	Who work as a cache for the page table.	A. TLB B. TLP C. LEB D. WAB
11	The principal of working of the cache memory largely depends on which locality.	A. Spatial locality B. Temporal locality C. Sequentially D. All of these
12	Cache is usually the _____ of memory access by the microprocessor.	A. First level B. Second level C. Third level D. Fourth level
13	The memory system is said to be effective if the access time of the cache is close to the effective access time of the.	A. ROM B. RAM C. HDD D. Processor
14	Second level is a cache on the	A. Main memory B. RAM C. Both a and b D. None

15	Who works as cache on the variable.	A. Memory B. Pointer C. Register D. Segment
16	The parity bits are used to check that a.	A. Two bit error B. Single bit error C. Multi bit error D. None
17	The index high order bits in the address known as.	A. Tags B. label C. Point D. Location
18	Inc case of direct mapped cache lower order line address bits are used the access the	A. RAM B. ROM C. Directory D. HDD
19	WA Stand for	A. Write allocate B. Wrote allocate C. Way allocate D. Word allocate
20	WB stand for	A. Write buffers B. Written buffers C. Wrote buffers D. None
21	EB stand for	A. Effect buffers B. Effecting buffers C. Effect ion buffers D. Eviction buffers
22	LRB stand for	A. Line ready buffers B. Line root buffers C. Line read buffers D. Line right buffers
23	LFB stand for	A. Line full buffers B. Line fill buffers C. Line fan buffers D. None
24	_____ is the most commonly used cache controller with a number of processor sets.	A. L 211 controller B. L 210 controller C. L 214 controller D. None
25	Microprocessor reference that are available in the cache are called.	A. Cache hits B. Cache line C. Cache misses D. Cache memory
26	FIFO stand for.	A. First first other B. First in first out C. First in firs over D. None
27	A fourth bit called the	A. Direct bit B. Cache bit C. Valid bit D. All of these
28	Direct mapping is a _____ to implement cache memory	A. Cheaper way B. Case way C. Cache way D. None
29	Which memory is used to holds the address of the data stored in the cache.	A. Associative memory B. Case memory C. Ordinary memory D. None
30	Which is the types of cache memory	A. Fully associative cache B. Direct mapped cache C. Set associative cache D. All of these