

## PPSC Computer Science Full Book test

| Sr | Questions                                                                                                 | Answers Choice                                                               |
|----|-----------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|
| 1  | Which multiplex by ADC 0808/0809                                                                          | A. 2:4<br>B. 3:8<br>C. 4:16<br>D. None                                       |
| 2  | Which chip is used for analogue to digital converter.                                                     | A. 0809<br>B. 0808<br>C. Both a and b<br>D. None                             |
| 3  | The time taken by the ADC from the active edge of SOC pulse till the active edge of EOC signal is called. | A. Conversion over<br>B. Conversion delay<br>C. Conversion signal<br>D. None |
| 4  | Which chip used for AD & DA converters in 8086 processor.                                                 | A. 8251<br>B. 8255<br>C. 8254<br>D. 8259                                     |
| 5  | 34 H& AX which operation is performed here                                                                | A. Input<br>B. Output<br>C. Progress<br>D. None                              |
| 6  | AL 7 99H which operation is performed here                                                                | A. Input<br>B. Out put<br>C. Both a and b<br>D. None                         |
| 7  | Which are used for port A in 8255 mode 1.                                                                 | A. PC0-PC2<br>B. PC3-PC7<br>C. PC6-PC7<br>D. PC3-PC5                         |
| 8  | Which are used for port B in 8255                                                                         | A. CPO-PC2<br>B. PC3-PC7<br>C. PC6-PC7<br>D. PC3-CP5                         |
| 9  | Which mode is used to double handshakes in 8255                                                           | A. Mode 0<br>B. Mode 1<br>C. Mode 2<br>D. Mode 3                             |
| 10 | Which mode is used for single handshake in 8255                                                           | A. Mode 0<br>B. Mode 1<br>C. Mode 2<br>D. None                               |
| 11 | Which is designed is automatically manage the handshake operation.                                        | A. 8251<br>B. 8254<br>C. 8255<br>D. 8259                                     |
| 12 | The proccesser of knowing the status of device and transferring the data with matching speeds is called.  | A. Handshaking<br>B. Peripheral<br>C. Ports<br>D. None                       |
| 13 | Which are used DMA controllers with 8085/8086 microprocessor.                                             | A. 8237<br>B. 8357<br>C. Both a and b<br>D. None                             |
| 14 | Which is widely used in interrupt controller with a number of microprocessor.                             | A. 8251<br>B. 8254<br>C. 8255<br>D. 8259                                     |
| 15 | Which programmable timer is used to generate timing signal                                                | A. 8255<br>B. 8254<br>C. 8251<br>D. 8259                                     |

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|----|-----------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 16 | Which is a programmable communication interface.                                              | A. 8255<br>B. 8254<br>C. 8251<br>D. 8359                                                                                                         |
| 17 | Which is the commonly used programmable interface and particular used to provide handshaking. | A. 8251<br>B. 8354<br>C. 8459<br>D. 8255                                                                                                         |
| 18 | DAC stand for                                                                                 | A. Analogue to analogue converters<br>B. Analogue to digital converters<br>C. Digital to digital converters<br>D. Digital to analogue converters |
| 19 | MEMER and MEMW means                                                                          | A. Memory read<br>B. Memory write<br>C. Both a and b<br>D. None                                                                                  |
| 20 | AEN stand for                                                                                 | A. Address enable<br>B. Address equivalent<br>C. Acknowledgment enable<br>D. Acknowledgment equivalent                                           |
| 21 | HR stand for.                                                                                 | A. Hold request<br>B. Hold read<br>C. Hold register<br>D. Hold resolver                                                                          |
| 22 | HLDA stand for                                                                                | A. High acknowledgment<br>B. Hold acknowledgement<br>C. High access<br>D. Hold access                                                            |
| 23 | OCW stand for                                                                                 | A. Operational command words<br>B. Operational conjunction words<br>C. Operational control words<br>D. Operational cost words                    |
| 24 | ICW stand for                                                                                 | A. interrupt command words<br>B. Interrupt command write<br>C. Initialization command words<br>D. Initialization command write                   |
| 25 | RD stand for                                                                                  | A. Read<br>B. Register<br>C. Request<br>D. Real                                                                                                  |
| 26 | INTA stand for                                                                                | A. Interrupt acknowledge<br>B. Interrupt access<br>C. Interrupt address<br>D. None                                                               |
| 27 | INT stand for                                                                                 | A. Input<br>B. Interrupt<br>C. Both a and b<br>D. None                                                                                           |
| 28 | IMR stand for                                                                                 | A. Input mask register<br>B. Input mask resolver<br>C. Interrupt mask resolver<br>D. Interrupt mask register                                     |
| 29 | PR stand for                                                                                  | A. Priority register<br>B. Priority resolver<br>C. Priority request<br>D. None                                                                   |
| 30 | ISR stand for                                                                                 | A. Interrupt service register<br>B. Input service register<br>C. In service register<br>D. All of these                                          |