CS-302 Quiz Preparation Virtual University

Sr	Questions	Answers Choice
1	A divide-by-50 counter divides the input _____ signal to a 1 Hz signal.	A. 10 Hz B. 50 Hz C. 100 Hz D. 500 Hz
2	Caveman number system is Base _____ number system	A. 2 B. 5 C. 10 D. 16
3	The output of an AND gate is one when _____	A. All of the inputs are one B. Any of the input is one C. Any of the input is zero D. All the inputs are zero
4	The storage cell in SRAM is	A. a flip –flop B. a capacitor C. a fuse D. a magnetic domain
5	The alternate solution for a demultiplexer-register combination circuit is _____	A. Parallel in / Serial out shift register B. Serial in / Parallel out shift register C. Parallel in / Parallel out shift register D. Serial in / Serial Out shift register
6	The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called _____	A. Radiation-Erase programming method (REPM) B. In-System Programming (ISP) C. In-chip Programming (ICP) D. Electronically-Erase programming method (EEPM)
7	The high density FLASH memory cell is implemented using _____	A. 1 floating-gate MOS transistor B. 2 floating-gate MOS transistors C. 4 floating-gate MOS transistors D. 6 floating-gate MOS transistors
8	The basic building block for a logical circuit is _____	A. A Flip-Flop B. A Logical Gate C. An Adder D. None of given options
9	The voltage gain of the Inverting Amplifier is given by the relation _____	A. Vout / Vin = - Rf / Ri B. Vout / Rf = - Vin / Ri C. Rf / Vin = - Ri / Vout D. Rf / Vin = Ri / Vout
10	For a gated D-Latch if EN=1 and D=1 then Q(t+1) = _____	A. 0 B. 1 C. Q(t) D. Invalid
11	Sum term (Max term) is implemented using _____ gates	A. OR B. AND C. NOT D. OR-AND
12	A positive edge-triggered flip-flop changes its state when _____	A. Low-to-high transition of clock B. High-to-low transition of clock C. Enable input (EN) is set D. Preset input (PRE) is set
13	At T0 the value stored in a 4-bit left shift was “1”. What will be the value of register after three clock pulses?	A. 2 B. 4 C. 6 D. 8
14	If the S and R inputs of the gated S-R latch are connected together using a _____gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)	A. AND B. OR C. NOT D. XOR
		A. Serial data to parallel

15	A multiplexer with a register circuit converts _____	B. Parallel data to serial C. Serial data to serial D. Parallel data to parallel
16	NAND gate is formed by connecting _____	A. AND Gate and then NOT Gate B. NOT Gate and then AND Gate C. AND Gate and then OR Gate D. OR Gate and then AND Gate
17	_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output	A. Resolution B. Accuracy C. Quantization D. Missing Code
18	Demultiplexer converts _____ data to _____ data.	A. Parallel data, serial data B. Serial data, parallel data C. Encoded data, decoded data D. All of the given options
19	A negative edge-triggered flip-flop changes its state when _____	A. Enable input (EN) is set B. Preset input (PRE) is set C. Low-to-high transition of clock D. High-to-low transition of clock
20	Consider an up/down counter that counts between 0 and 15, if external input(X) is “0” the counter counts upward (0000 to 1111) and if external input (X) is “1” the counter counts downward (1111 to 0000), now suppose that the present state is “1100” and X=1, the next state of the counter will be _____	A. 0000 B. 1101 C. 1011 D. 1111