CS-302 Quiz Preparation Virtual University

Sr	Questions	Answers Choice
1	We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____	A. Using S-R Flop-Flop B. D-flipflop C. J-K flip-flop D. T-Flip-Flop
2	A positive edge-triggered flip-flop changes its state when _____	A. Low-to-high transition of clock B. High-to-low transition of clock C. Enable input (EN) is set D. Preset input (PRE) is set
3	Generally, the Power dissipation of _____ devices remains constant throughout their operation.	A. TTL B. CMOS 3.5 series C. CMOS 5 Series D. Power dissipation of all circuits increases with time
4	The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called _____	A. Radiation-Erase programming method (REPM) B. In-System Programming (ISP) C. In-chip Programming (ICP) D. Electronically-Erase programming method (EEPM)
5	The output of an AND gate is one when _____	A. All of the inputs are one B. Any of the input is one C. Any of the input is zero D. All the inputs are zero
6	The sequence of states that are implemented by a n-bit Johnson counter is	A. n+2 (n plus 2) B. 2n (n multiplied by 2) C. 2n (2 raise to power n) D. n2 (n raise to power 2)
7	_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.	A. Race condition B. Clock Skew C. Ripple Effect D. None of given options
8	Excess-8 code assigns _____ to “+7”	A. 0000 B. 1001 C. 1000 D. 1111
9	In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.	A. Moore machine B. Mealy machine C. Johnson counter D. Ring counter
10	The simplest and most commonly used Decoders are the _____ Decoders	A. (n-1) to (2n-1) B. (n-1) to 2n C. n to 2n-1 D. n to 2n
11	A synchronous decade counter will have _____ flip-flops	A. 3 B. 4 C. 7 D. 10
12	Smallest unit of binary data is a _____	A. Bit B. Nibble C. Byte D. Word
13	The best state assignment tends to _____.	A. Maximizes the number of state variables that don’t change in a group of related states B. Minimizes the number of state variables that don”t change in a group of related states C. Minimize the equivalent states D. None of given options
14	NAND gate is formed by connecting	A. AND Gate and then NOT Gate B. NOT Gate and then AND Gate

	_____	C. AND Gate and then OR Gate D. OR Gate and then AND Gate
15	A GAL is essentially a _____.	A. Non-reprogrammable PAL B. PAL that is programmed only by the manufacturer C. Very large PAL D. Reprogrammable PAL
16	_____ counters as the name indicates are not triggered simultaneously.	A. Asynchronous B. Synchronous C. Positive-Edge triggered D. Negative-Edge triggered
17	The address from which the data is read, is provided by _____	A. Depends on circuitry B. None of given options C. RAM D. Microprocessor
18	Above is the circuit diagram of _____.	A. Asynchronous up-counter B. Asynchronous down-counter C. Synchronous up-counter D. Synchronous down-counter
19	A full-adder has a Cin = 0. What are the sum (<PRIVATE "TYPE=PICT;ALT=sigma">) and the carry (Cout) when A = 1 and B = 1?	A. = 0, Cout = 0 B. = 0, Cout = 1 C. = 1, Cout = 0 D. = 1, Cout = 1
20	NOR gate is formed by connecting _____	A. OR Gate and then NOT Gate B. NOT Gate and then OR Gate C. AND Gate and then OR Gate D. OR Gate and then AND Gate