

CS-302 Quiz Preparation Virtual University

Sr	Questions	Answers Choice
1	In _____ outputs depend only on the current state	A. Mealy machine B. Moore Machine C. State Reduction table D. State Assignment table
2	In a sequential circuit the next state is determined by _____ and _____	A. State variable, current state B. Current state, flip-flop output C. Current state and external input D. Input and clock signal applied
3	THE HOURS COUNTER IS IMPLEMENTED USING _____	A. ONLY A SINGLE MOD-12 COUNTER IS REQUIRED B. MOD-10 AND MOD-6 COUNTERS C. MOD-10 AND MOD-2 COUNTERS D. A SINGLE DECADE COUNTER AND A FLIP-FLOP
4	The _____ input overrides the _____ input.	A. Asynchronous, synchronous B. Synchronous, asynchronous C. Preset input (PRE), Clear input (CLR) D. Clear input (CLR), Preset input (PRE)
5	If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be	A. set B. reset C. invalid D. clear
6	We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____	A. Using S-R Flop-Flop B. D-flipflop C. J-K flip-flop D. T-Flip-Flop
7	$(A + B)(A + B + C)(A + C)$ is an example of _____	A. Product of sum form B. Sum of product form C. Demorgans law D. Associative law
8	_____ is one of the examples of asynchronous inputs.	A. J-K input B. S-R input C. D input D. Clear Input (CLR)
9	_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.	A. Resolution B. Missing Code C. Accuracy D. Quantization
10	_____ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.	A. Race condition B. Clock Skew C. Ripple Effect D. None of given options
11	_____ is one of the examples of synchronous inputs.	A. J-K input B. EN input C. Preset input (PRE) D. Clear Input (CLR)
12	The _____ input overrides the _____ input	A. Asynchronous, synchronous B. Synchronous, asynchronous C. Preset input (PRE), Clear input (CLR) D. Clear input (CLR), Preset input (PRE)
13	The output of the expression $F=A.B.C$ will be Logic _____ when $A=1, B=0, C=1$	A. Undefined B. One C. Zero D. No Output as input is invalid
14	_____ is invalid number of cells in a single group formed by the adjacent cells in K-map	A. 2 B. 8 C. 12 D. 16

15	The storage cell in SRAM is	A. a flip-flop B. a capacitor C. a fuse D. a magnetic domain
16	74HC163 has two enable input pins which are _____ and _____	A. ENP, ENT B. ENI, ENC C. ENP, ENC D. ENT, ENI
17	Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state	A. Ten B. Eight C. Three D. Two
18	The simplest and most commonly used Decoders are the _____ Decoders	A. n to $2n-1$ B. n to 2^n C. (n-1) to 2^n D. (n-1) to $(2n-1)$
19	$Q_2 := Q_1 \text{ OR } X \text{ OR } Q_3$	A. $Q_2 := Q_1 \oplus X \oplus Q_3$ B. $Q_2 := Q_1 \oplus X \oplus Q_3$ C. $Q_2 := Q_1 \& X \& Q_3$ D. $Q_2 := Q_1 \& X \& Q_3$
20	In _____ the Q output of the last flip-flop of the shift register is connected to the data input of the first flipflop.	A. Moore machine B. Meally machine C. Johnson counter D. Ring counter