CS-302 Quiz Preparation Virtual University

Sr	Questions	Answers Choice
1	LUT is acronym for _____	A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options
2	The low to high or high to low transition of the clock is considered to be a(n) _____.	A. State B. Edge C. Trigger D. One-shot
3	Flip flops are also called _____	A. Bi-stable dualvibrators B. Bi-stable transformer C. Bi-stable multivibrators D. Bi-stable singlevibrators
4	_____ is used to simplify the circuit that determines the next state.	A. State diagram B. Next state table C. State reduction D. State assignment
5	The divide-by-60 counter in digital clock is implemented by using two cascading counters:	A. Mod-6, Mod-10 B. Mod-50, Mod-10 C. Mod-10, Mod-50 D. Mod-50, Mod-6
6	The simplest and most commonly used Decoders are the _____ Decoders	A. (n-1) to (2n-1) B. (n-1) to 2n C. n to 2n-1 D. n to 2n
7	Stack is an acronym for_____	A. FIFO memory B. LIFO memory C. Flash Memory D. Bust Flash Memory
8	NOR gate is formed by connecting _____	A. OR Gate and then NOT Gate B. NOT Gate and then OR Gate C. AND Gate and then OR Gate D. OR Gate and then AND Gate
9	In _____ outputs depend only on the current state	A. Mealy machine B. Moore Machine C. State Reduction table D. State Assignment table
10	If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop	A. 0 B. 1 C. Invalid D. Input is invalid
11	LUT is acronym for _____.	A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options
12	The address from which the data is read, is provided by _____	A. Depends on circuitry B. None of given options C. RAM D. Microprocessor
13	_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.	A. Resolution B. Missing Code C. Accuracy D. Quantization
14	The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called _____	A. Radiation-Erase programming method (REPM) B. In-System Programming (ISP) C. In-chip Programming (ICP) D. Electronically-Erase programming method (EEPM)
15	Generally, the Power dissipation of devices remains constant throughout their	A. TTL B. CMOS 3.5 series

15	operation.	C. CMOS 5 Series D. Power dissipation of all circuits increases with time
16	Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)	A. 1100 B. 0011 C. 0000 D. 1111
17	(A + B)(A + B + C)(A + C) is an example of _____	A. Product of sum form B. Sum of product form C. Demorgans law D. Associative law
18	A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status	A. 3 B. 7 C. 8 D. 15
19	Addition of two octal numbers “36” and “71” results in _____	A. 213 B. 123 C. 127 D. 345
20	_____ is said to occur when multiple internal variables change due to change in one input variable.	A. Clock Skew B. Race condition C. Hold delay D. Hold and Wait
21	FIFO is an acronym for _____	A. First In, First Out B. Fly in, Fly Out C. Fast in, Fast Out D. None of given options
22	The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms	A. 4 B. 8 C. 12 D. 16
23	The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?	A. A > B = 1, A < B = 0, A < B = 1 B. A > B = 0, A < B = 1, A = B = 0 C. A > B = 1, A < B = 0, A = B = 0 D. A > B = 0, A < B = 1, A = B = 1
24	A transparent mode means _____.	A. The changes in the data at the inputs of the latch are seen at the output B. The changes in the data at the inputs of the latch are not seen at the output C. Propagation Delay is zero (Output is immediately changed when clock signal is applied) D. Input Hold time is zero (no need to maintain input after clock transition)
25	A divide-by-50 counter divides the input _____ signal to a 1 Hz signal.	A. 10 Hz B. 50 Hz C. 100 Hz D. 500 Hz
26	A positive edge-triggered flip-flop changes its state when _____	A. Low-to-high transition of clock B. High-to-low transition of clock C. Enable input (EN) is set D. Preset input (PRE) is set
27	_____ is invalid number of cells in a single group formed by the adjacent cells in K-map	A. 2 B. 8 C. 12 D. 16
28	A GAL is essentially a _____.	A. Non-reprogrammable PAL B. PAL that is programmed only by the manufacturer C. Very large PAL D. Reprogrammable PAL
29	RCO Stands for _____	A. Reconfiguration Counter Output B. Reconfiguration Clock Output C. Ripple Counter Output D. Ripple Clock Output
30	The alternate solution for a demultiplexer-register combination circuit is _____	A. Parallel in / Serial out shift register B. Serial in / Parallel out shift register C. Parallel in / Parallel out shift register D. Serial in / Serial Out shift register

		D. Serial In / Serial Out shift register
31	A synchronous decade counter will have _____ flip-flops.	A. 3 B. 4 C. 7 D. 10
32	"A + B = B + A" is _____	A. Demorgan"s Law B. Distributive Law C. Commutative Law D. Associative Law
33	Excess-8 code assigns _____ to “+7”	A. 0000 B. 1001 C. 1000 D. 1111
34	The OR Gate performs a Boolean _____ function	A. Addition B. Subtraction C. Multiplication D. Division
35	For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs will_____ if the clock goes HIGH	A. toggle B. set C. reset D. not change
36	THE HOURS COUNTER IS IMPLEMENTED USING _____	A. ONLY A SINGLE MOD-12 COUNTER IS REQUIRED B. MOD-10 AND MOD-6 COUNTERS C. MOD-10 AND MOD-2 COUNTERS D. A SINGLE DECADE COUNTER AND A FLIP-FLOP
37	A frequency counter _____	A. Counts pulse width B. Counts no. of clock pulses in 1 second C. Counts high and low range of given clock pulse D. None of given options
38	When the control line in tri-state buffer is high the buffer operates like a _____gate	A. AND B. OR C. NOT D. XOR
39	LUT is acronym for _____	A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options
40	In a sequential circuit the next state is determined by _____ and _____	A. State variable, current state B. Current state, flip-flop output C. Current state and external input D. Input and clock signal applied
41	The basic building block for a logical circuit is _____	A. A Flip-Flop B. A Logical Gate C. An Adder D. None of given options
42	The design and implementation of synchronous counters start from _____	A. Truth table B. state diagram C. k-map D. state table
43	Excess-8 code assigns _____ to “-8”	A. 1110 B. 1100 C. 1000 D. 0000
44	in _____, all the columns in the same row are either read or written.	A. Sequential Access B. MOS Access C. FAST Mode Page Access D. None of given options
45	The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines	A. Write Time B. Recycle Time C. Refresh Time D. Access Time
46	Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse?	A. 1100 B. 0011 C. 0000 D. 1111
47	Demultiplexer is also called.	A. Data selector B. Data router C. Data distributor D. Data encoder

		D. Data encoder
48	The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines.	A. Write Time B. Recycle Time C. Refresh Time D. Access Time
49	If the FIFO Memory output is already filled with data then _____	A. It is locked; no data is allowed to enter B. It is not locked; the new data overwrites the previous data. C. Previous data is swapped out of memory and new data enters D. None of given options
50	In asynchronous transmission when the transmission line is idle, _____	A. It is set to logic low B. Remains in previous state C. It is set to logic high D. State of transmission line is not used to start transmission
51	Determine the values of A, B, C, and D that make the sum term A(bar) + B+C(bar)+D equal to zero.	A. A = 1, B = 0, C = 0, D = 0 B. A = 1, B = 0, C = 1, D = 0 C. A = 0, B = 1, C = 0, D = 0 D. A = 1, B = 0, C = 1, D = 1
52	We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____	A. Using S-R Flop-Flop B. D-flipflop C. J-K flip-flop D. T-Flip-Flop
53	A negative edge-triggered flip-flop changes its state when _____	A. Enable input (EN) is set B. Preset input (PRE) is set C. Low-to-high transition of clock D. High-to-low transition of clock
54	In a state diagram, the transition from a current state to the next state is determined by.	A. Current state and the inputs B. Current state and outputs C. Previous state and inputs D. Previous state and outputs
55	_____ is one of the examples of synchronous inputs.	A. J-K input B. EN input C. Preset input (PRE) D. Clear Input (CLR)
56	_____ is used to minimize the possible no. of states of a circuit.	A. State assignment B. State reduction C. Next state table D. State diagram
57	The simplest and most commonly used Decoders are the _____ Decoders	A. n to 2n-1 B. n to 2n C. (n-1) to 2n D. (n-1) to (2n-1)
58	A multiplexer with a register circuit converts _____	A. Serial data to parallel B. Parallel data to serial C. Serial data to serial D. Parallel data to parallel
59	DRAM stands for _____	A. Dynamic RAM B. Data RAM C. Demoduler RAM D. None of given options
60	The power dissipation, PD, of a logic gate is the product of the	A. dc supply voltage and the peak current B. dc supply voltage and the average supply current C. ac supply voltage and the peak current D. ac supply voltage and the average supply current
61	The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.	A. Set-up time B. Hold time C. Pulse Interval time D. Pulse Stability time
62	The alternate solution for a multiplexer and a register circuit is _____	A. Parallel in / Serial out shift register B. Serial in / Parallel out shift register C. Parallel in / Parallel out shift register D. Serial in / Serial Out shift register
63	The ANSI/IEEE Standard 754 defines a _____Single-Precision Floating Point format for binary numbers.	A. 8-bit B. 16-bit C. 32-bit D. 64-bit

		D. 64-bit
64	A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is	A. 10 mW B. 25 mW C. 64 mW D. 1024
65	The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder	A. AND B. OR C. NOT D. XOR
66	Smallest unit of binary data is a _____	A. Bit B. Nibble C. Byte D. Word
67	In a sequential circuit the next state is determined by _____ and _____.	A. State variable, current state B. Current state, flip-flop output C. Current state and external input D. Input and clock signal applied
68	A positive edge-triggered flip-flop changes its state when _____	A. Low-to-high transition of clock B. High-to-low transition of clock C. Enable input (EN) is set D. Preset input (PRE) is set
69	The output of an AND gate is one when _____	A. All of the inputs are one B. Any of the input is one C. Any of the input is zero D. All the inputs are zero
70	5-bit Johnson counter sequences through ____ states	A. 7 B. 10 C. 32 D. 25
71	The _____ Encoder is used as a keypad encoder.	A. 2-to-8 encoder B. 4-to-16 encoder C. BCD-to-Decimal D. Decimal-to-BCD Priority
72	WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO.	A. THE FLOP-FLOP IS TRIGGERED B. Q=0 AND Q"=1 C. Q=1 AND Q'=0 D. THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED
73	The best state assignment tends to _____.	A. Maximizes the number of state variables that don't change in a group of related states B. Minimizes the number of state variables that don"t change in a group of related states C. Minimize the equivalent states D. None of given options
74	74HC163 has two enable input pins which are _____ and _____.	A. ENP, ENT B. ENI, ENC C. ENP, ENC D. ENT, ENI
75	Q2 :=Q1 OR X OR Q3 The above ABEL expression will be	A. Q2:= Q1 $ X $ Q3 B. Q2:= Q1 # X # Q3 C. Q2:= Q1 & X & Q3 D. Q2:= Q1 ! X ! Q3
76	Above is the circuit diagram of _____.	A. Asynchronous up-counter B. Asynchronous down-counter C. Synchronous up-counter D. Synchronous down-counter
77	Demultiplexer converts _____ data to _____ data.	A. Parallel data, serial data B. Serial data, parallel data C. Encoded data, decoded data D. All of the given options
78	The output of the expression F=A.B.C will be Logic _____ when A=1, B=0, C=1	A. Undefined B. One C. Zero D. No Output as input is invalid
79	In _____ the Q output of the last flip-flop of the shift register is connected to the data input of the first flipflop.	A. Moore machine B. Meally machine C. Johnson counter D. Ring counter
80	The 4-bit 2"s complement representation of "+5" is	A. 1010 B. 1110

	The 4-bit 2's complement representation of -3 is _____	C. 1011 D. 0101
81	Q2 :=Q1 OR X OR Q3	A. Q2:= Q1 $ X $ Q3 B. Q2:= Q1 # X # Q3 C. Q2:= Q1 & X & Q3 D. Q2:= Q1 ! X ! Q3
82	_____ is used to minimize the possible no. of states of a circuit.	A. State assignment B. State reduction C. Next state table D. State diagram
83	An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is _____	A. Using a single comparator B. Using Iterative Circuit based Comparators C. Connecting comparators in vertical hierarchy D. Extra logic gates are always required
84	FIFO is an acronym for _____	A. First In, First Out B. Fly in, Fly Out C. Fast in, Fast Out D. None of given options
85	The sequence of states that are implemented by a n-bit Johnson counter is	A. n+2 (n plus 2) B. 2n (n multiplied by 2) C. 2n (2 raise to power n) D. n2 (n raise to power 2)
86	The OR gate performs Boolean _____.	A. multiplication B. subtraction C. division D. addition
87	Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer	A. A parallel to serial converter circuit B. A counter circuit C. A BCD to Decimal decoder D. A 2-to-8 bit decoder
88	If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop	A. 0 B. 1 C. Invalid D. Input is invalid
89	The design and implementation of synchronous counters start from _____	A. state table B. k-map C. state diagram D. Truth table
90	74HC163 has two enable input pins which are _____ and _____	A. ENP, ENT B. ENI, ENC C. ENP, ENC D. ENT, ENI
91	_____ is one of the examples of asynchronous inputs.	A. J-K input B. S-R input C. D input D. Clear Input (CLR)
92	NAND gate is formed by connecting _____	A. AND Gate and then NOT Gate B. NOT Gate and then AND Gate C. AND Gate and then OR Gate D. OR Gate and then AND Gate
93	In a state diagram, the transition from a current state to the next state is determined by	A. Current state and the inputs B. Current state and outputs C. Previous state and inputs D. Previous state and outputs
94	In the following statement Z PIN 20 ISTYPE „reg.invert"; The keyword "reg.invert" indicates _____	A. An inverted register input B. An inverted register input at pin 20 C. Active-high Registered Mode output D. Active-low Registered Mode output
95	The process of converting the analogue signal into a digital representation (code) is known as _____	A. Strobing B. Amplification C. Quantization D. Digitization
96	Consider A=1,B=0,C=1. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be _____	A. Zero B. One C. Undefined D. No output as input is invalid
		A. 1 floating-gate MOS transistor

97	The high density FLASH memory cell is implemented using _____	B. 2 floating-gate MOS transistors C. 4 floating-gate MOS transistors D. 6 floating-gate MOS transistors
98	The output of an XNOR gate is 1 when _____ . I) All the inputs are zero II) Any of the inputs is zero III) Any of the inputs is one IV) All the inputs are one.	A. I Only B. IV Only C. I and IV only D. II and III only
99	_____ counters as the name indicates are not triggered simultaneously.	A. Asynchronous B. Synchronous C. Positive-Edge triggered D. Negative-Edge triggered
100	For a gated D-Latch if EN=1 and D=1 then Q(t+1) = _____	A. 0 B. 1 C. Q(t) D. Invalid
101	In asynchronous transmission when the transmission line is idle, _____	A. It is set to logic low B. It is set to logic high C. Remains in previous state D. State of transmission line is not used to start transmission
102	_____ is said to occur when multiple internal variables change due to change in one input variable	A. Clock Skew B. Race condition C. Hold delay D. Hold and Wait
103	_____ is one of the examples of synchronous inputs	A. J-K input B. EN input C. Preset input (PRE) D. Clear Input (CLR)
104	The output of an XOR gate is zero (0) when _____ I) All the inputs are zero II) Any of the inputs is zero III) Any of the inputs is one IV) All the inputs are one.	A. I Only B. IV Only C. I and IV only D. II and III only
105	_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.	A. Race condition B. Clock Skew C. Ripple Effect D. None of given options
106	The storage cell in SRAM is	A. a flip –flop B. a capacitor C. a fuse D. a magnetic domain
107	In order to synchronize two devices that consume and produce data at different rates, we can use _____	A. Read Only Memory B. Fist In First Out Memory C. Flash Memory D. Fast Page Access Mode Memory
108	The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____	A. Doesn't have an invalid state B. Sets to clear when both J = 0 and K = 0 C. It does not show transition on change in pulse D. It does not accept asynchronous inputs
109	The _____ input overrides the _____ input.	A. Asynchronous, synchronous B. Synchronous, asynchronous C. Preset input (PRE), Clear input (CLR) D. Clear input (CLR), Preset input (PRE)
110	LUT is acronym for _____.	A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options
111	74HC163 has two enable input pins which are _____ and _____	A. ENP, ENT B. ENI, ENC C. ENP, ENC D. ENT, ENI
112	The total amount of memory that is supported by any digital system depends upon _____	A. The organization of memory B. The structure of memory C. The size of decoding unit D. The size of the address bus of the microprocessor
113	In asynchronous transmission when the transmission line is idle	A. It is set to logic low B. It is set to logic high C. Remains in previous state

113	In asynchronous transmission when the transmission line is idle, _____	C. Remains in previous state D. State of transmission line is not used to start transmission
114	The decimal “17” in BCD will be represented as _____10001(right opt is not given)	A. 11101 B. 11101 C. 10111 D. 11110
115	A logic circuit with an output consists of _____	A. two AND gates, two OR gates, two inverters B. three AND gates, two OR gates, one inverter C. two AND gates, one OR gate, two inverters D. two AND gates, one OR gate
116	A synchronous decade counter will have _____ flip-flops	A. 3 B. 4 C. 7 D. 10
117	_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output	A. Resolution B. Accuracy C. Quantization D. Missing Code
118	A positive edge-triggered flip-flop changes its state when _____	A. Low-to-high transition of clock B. High-to-low transition of clock C. Enable input (EN) is set D. Preset input (PRE) is set
119	At T0 the value stored in a 4-bit left shift was “1”. What will be the value of register after three clock pulses?	A. 2 B. 4 C. 6 D. 8
120	In _____ outputs depend only on the combination of current state and inputs.	A. Mealy machine B. Moore Machine C. State Reduction table D. State Assignment table
121	A decade counter is _____.	A. Mod-3 counter B. Mod-5 counter C. Mod-8 counter D. Mod-10 counter
122	In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.	A. Moore machine B. Meally machine C. Johnson counter D. Ring counter
123	Given the state diagram of an up/down counter, we can find _____	A. The next state of a given present state B. The previous state of a given present state C. Both the next and previous states of a given state D. The state diagram shows only the inputs/outputs of a given states
124	Consider an up/down counter that counts between 0 and 15, if external input(X) is “0” the counter counts upward (0000 to 1111) and if external input (X) is “1” the counter counts downward (1111 to 0000), now suppose that the present state is “1100” and X=1, the next state of the counter will be _____	A. 0000 B. 1101 C. 1011 D. 1111
125	If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be	A. set B. reset C. invalid D. clear
126	A Nibble consists of _____ bits	A. 2 B. 8 C. 4 D. 16
127	A positive edge-triggered flip-flop changes its state when _____.	A. Low-to-high transition of clock B. High-to-low transition of clock C. Enable input (EN) is set D. Preset input (PRE) is set
128	A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.	A. 3 B. 7 C. 8 D. 15
129	What is the difference between a D latch and a D flip-flop?	A. The D latch has a clock input B. The D flip-flop has an enable input C. The D latch is used for faster

		operation D. The D flip-flop has a clock input
130	A 8-bit serial in / parallel out shift register contains the value “8”, _____ clock signal(s) will be required to shift the value completely out of the register.	A. 1 B. 2 C. 4 D. 8
131	The decimal “17” in BCD will be represented as _____	A. ₁₁₁₀₁ B. 11011 C. 10111 D. 11110
132	The voltage gain of the Inverting Amplifier is given by the relation _____	A. Vout / Vin = - Rf / Ri B. Vout / Rf = - Vin / Ri C. Rf / Vin = - Ri / Vout D. Rf / Vin = Ri / Vout
133	Stack is an acronym for _____	A. FIFO memory B. LIFO memory C. Flash Memory D. Bust Flash Memory
134	Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state	A. Ten B. Eight C. Three D. Two
135	The _____ input overrides the _____ input	A. Asynchronous, synchronous B. Synchronous, asynchronous C. Preset input (PRE), Clear input (CLR) D. Clear input (CLR), Preset input (PRE)
136	Sum term (Max term) is implemented using _____ gates	A. OR B. AND C. NOT D. OR-AND
137	THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING A _____	A. GATED FLIP-FLOPS B. PULSE TRIGGERED FLIP-FLOPS C. POSITIVE-EDGE TRIGGERED FLIP-FLOPS D. NEGATIVE-EDGE TRIGGERED FLIP-FLOPS
138	In designing any counter the transition from a current state to the next sate is determined by	A. Current state and inputs B. Only inputs C. Only current state D. current state and outputs
139	If the S and R inputs of the gated S-R latch are connected together using a _____gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)	A. AND B. OR C. NOT D. XOR
140	Which is not characteristic of a shift register?	A. Serial in/parallel in B. Serial in/parallel out C. Parallel in/serial out D. Parallel in/parallel out
141	3.3 v CMOS series is characterized by _____ and _____as compared to the 5 v CMOS series	A. Low switching speeds, high power dissipation B. Fast switching speeds, high power dissipation C. Fast switching speeds, very low power dissipation D. Low switching speeds, very low power dissipation
142	The expression F=A+B+C describes the operation of three bits _____ Gate	A. OR B. AND C. NOT D. NAND
143	The ABEL symbol for “OR” operation is	A. ! B. & C. # D. $
144	The divide-by-60 counter in digital clock is implemented by using two cascading counters	A. Mod-6, Mod-10 B. Mod-50, Mod-10 C. Mod-10, Mod-50 D. Mod-50, Mod-6
145	Caveman number system is Base _____ number system	A. 2 B. 5 C. 10

		D. 16
146	The three fundamental gates are _____	A. AND, NAND, XOR B. OR, AND, NAND C. NOT, NOR, XOR D. NOT, OR, AND
147	A full-adder has a Cin = 0. What are the sum (<PRIVATE "TYPE=PICT;ALT=sigma">) and the carry (Cout) when A = 1 and B = 1?	A. = 0, Cout = 0 B. = 0, Cout = 1 C. = 1, Cout = 0 D. = 1, Cout = 1