PPSC Computer Science Topic 17 Microprocessor And Assembly Language

Sr	Questions	Answers Choice
1	Which is the components of microprocessor.	A. Register unit B. Arithmetic and logical unit C. Timing and control unit D. All of these
2	IMR stand for	A. Input mask register B. Input mask resolver C. Interrupt mask resolver D. Interrupt mask register
3	RISC stand for.	A. Reduced instruction set computer B. Reduced instruct set compare C. Reduce instruction stand computer D. All of these
4	the CPU Sends out a _____ signal to indicate that valid data is available on the data bus.	A. READ B. WRITE C. Both a and b D. None
5	How many group of memory unit.	A. three B. Two C. Four D. One
6	BP stand for	A. Bit pointer B. Base pointer C. Bus pointer D. Byte pointer
7	A central processing unit fabricated on a single chip of semiconductor is called.	A. RAM B. ROM C. Microprocessor D. None
8	MOC stand for	A. Memory operation complex B. Micro operation complex C. Memory operation complete D. None
9	There are primarily two types of register	A. General purpose register B. Dedicated register C. a and b D. None
10	FIFO stand for.	A. First first other B. First in first out C. First in firs over D. None
11	The external device is connected to a pin called the__ pin on the processor chip.	A. Interrupt B. Transfer C. Both D. None
12	The act of acquiring an instruction is referred as the ____ the instruction	A. Fetching B. Fetch cycle C. Botha a and b D. None
13	Power PC microprocessor architecture is developed by.	A. Apple B. IBM C. Motorola D. All these
14	Which chip is used for analogue to digital converter.	A. 0809 B. 0808 C. Both a and b D. None
15	8254 counters can count in the	A. Binary B. Decimal C. Hexadecimal

		D. Both a and b
16	Which register contains the 8086/8088 flag	A. Status register B. Stack register C. Flag register D. Stand register
17	a 16 bit address bus can generate _____ address bus.	A. 16 B. 32 C. 36 D. 64
18	Which storage technique does not decoding circuit.	A. Linear decoding B. Fully decoding C. partially D. None
19	Which are the cache controller ports.	A. 64 bit AHB -Lite slave ports B. 64- bit AHB -Lite Master ports C. Both a and b D. None
20	BCD stand for	A. Binary coded decimal B. Binary coded decoded C. Both a and b D. None